US-PAT-NO: 5903544

DOCUMENT-IDENTIFIER: US 5903544 A

TITLE: Packet handler

DATE-ISSUED: May 11, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sakamoto; Ken'ichi	Tokyo	N/A	N/A	JP
Shinohara; Yasunari	Kawasaki	N/A	N/A	JP
Kozaki; Takahiko	Tokyo	N/A	N/A	JP

US-CL-CURRENT: 370/218, 370/220 , 370/419

ABSTRACT:

A packet handler includes an interface circuit of an ATM handler corresponding in one-to-one relation to each input/output port of an ATM switch. A switch interface including a disconnection circuit and a distribution circuit controls the cell flow from each interface circuit to a corresponding input port and the cell from the output ports of the ATM switch to each interface circuit. In a set of interface circuits, one redundant transmission path can be replaced arbitrarily with two nonredundant independent
transmission paths. The ATM communication system can thus accommodate redundant transmission paths and nonredundant transmission paths in an arbitrary ratio.

12 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Application Filing Date - AD (1):
19970403

Detailed Description Text - DETX (9):

The write **control** circuit writes each input cell paired with a pointer address, for example, in the **common buffer memory,** and stores the pointer address paired with an output port in an address table. The write address table is accessed on the basis of the routing information of each new input **cell** each time such a new input **cell** is supplied thereby to read the **last** pointer address for each output port specified by the routing information. With the **last** pointer address as a write address, the input **cell** and the new pointer address retrieved from a vacant address buffer are written in the common buffer memory. In this way, a logic queue buffer can be formed in which
the input cells are linked sequentially by pointers for each output port.

interface circuits 3 and the ATM switch common part 4 through a control transfer path 10. In FIG. 1, each interface circuit 3 is shown in a block. In an actual handler, however, as described later with reference to FIG. 5, the interface circuit 3 includes an input line interface 3*a* connected to an input line and an output line interface 3*b* connected to an output line, each having the physical layer processing function and the ATM layer processing function.

The ATM switch common part 4 includes an ATM switch 5 having a plurality of input ports I (I-1 to I-n) and a plurality of output ports O (O-1 to O-n), and a plurality of switch interfaces 6 each having two input ports and two output ports as a set.

In the ATM handler according to this embodiment, the number of the interface circuits 3 corresponds to the number of input/output ports of the ATM switch. Each switch interface 6 includes a disconnection circuit 7 inserted between a set of input ports I-i, I-(i+1) and two input line interfaces 3*a* connected to two transmission paths 2-i, 2-(i+1), respectively, and a distribution circuit 8 arranged between a set of output ports O-i, O-(i+1) and two output line interfaces 3*b* connected to the transmission paths 2-i, 2-(i+1), respectively.

The functions of the disconnection circuit 7 and the distribution circuit 8 will be explained with reference to FIGS. 5A and 5B. In FIGS. 5A and 5B, the solid lines show the X signal flow, and the marks indicate the signals being disconnected.

FIG. 5A shows the status of the switch interface 6 with two interface circuits 3 accommodating nonredundant paths. In this case, the disconnection circuit 7 supplies the input cells from the input line interfaces 3*a*-i, 3*a*-(i+1) without blocking to the two input ports I-i, I-(i+1) of the ATM switch 5.

The ATM switch 5, as proposed in JP-A-4-276943, for example, is of a common buffer type. In the ATM switch of common buffer type, the input cells supplied concurrently from a plurality of input ports are rearranged into temporal cell streams by a multiplexer and sequentially accumulated in a queue buffer corresponding to the output ports formed in the common buffer memory by a write control circuit. In order to read the cells from the common buffer memory, the queue buffer is accessed in the order of the output ports by a read control circuit, so that the leading cells of each queue buffer are read and sequentially distributed among the corresponding output ports by a demultiplexer. The write control circuit and the read control circuit alternately access the common buffer memory.

The write control circuit writes each input cell paired with a pointer address, for example, in the common buffer memory, and stores the pointer address paired with an output port in an address table. The write address table is accessed on the basis of the routing information of each new input cell each time such a new input cell is supplied thereby to read the last pointer address for each output port specified by the routing information. With the last pointer address as a write address, the input cell and the new pointer address retrieved from a vacant address buffer are written in the common buffer memory. In this way, a logic queue buffer can be formed in which the input cells are linked sequentially by pointers for each output port.

The read control circuit stores a pointer address corresponding to each output port in the read address table, the pointer addresses are read from the table in the order of the output ports. With this pointer address as a read address, the cells are read out of the common buffer memory. In the process, the pointer addresses read with the cells are stored in the read address table. These pointer addresses are used as read addresses for the queue buffer at the next time point of outputting the cells to the corresponding output ports. The pointer addresses that have been used as a read address are registered as vacant addresses in the vacant address buffer.

In FIG. 5A, numerals 20-i and 20-(i+1) designate queue buffers formed in the common buffer memory of the ATM switch 5 and correspond to the output ports O-i and O-(i+1), respectively. The cells (output cells) retrieved from these queue buffers are supplied through the distribution circuit 8 to the output line interfaces 3*b*-i, 3*b*-(i+1), respectively, and after removing the internal cell information therefrom, are sent out to the transmission paths (output lines).

FIGS. 5B and 5C show the status of the switch interface 6 with redundant paths accommodated in the interface circuit.

FIG. 5B refers to the case in which the transmission path 2-i is an active path, and FIG. 5C the case in which the transmission path 2-(i+1) is an active path.

According to this embodiment, as evident from FIG. 5C, for example, the output signal from one of a pair of input line interfaces 3*a*-i and 3*a*-(i+1), i.e., the input line interface 3*a*-i for active path, is applied through the disconnection circuit 7 to the input port I-i of the ATM switch 5, while the output signal from the input line interface 3*a*-(i+1) for standby path is blocked by the disconnection circuit so that the input port I-(i+1) remains unused.

The ATM switch 5 forms a queue buffer 20-i corresponding to the output port 0-i connected to the output line 2-i constituting one of the redundant output lines. The output cells retrieved from the queue buffer 20-i are supplied to a pair of output line interfaces 3*b*-i, 3*b*-(i+1) through the distribution circuit 8, thereby sending out the same signal (cell) to the redundant transmission paths 2-i, 2-(i+1).

FIG. 6 shows the switch interface 6 including the disconnection circuit 7 and the distribution circuit 8 according to an embodiment. The input signal wire from the interface circuit 3-i is designated as 34-0, the input signal wire from the interface circuit 3-(i+1) as 34-1, the output signal to the interface circuit 3-i as 35-0, and the output signal line to the interface circuit 3-(i+1) as 35-1.

The disconnection circuit 7 includes AND gates 32-0 and 32-1 each supplied with one of the signals from the input signal wires 34-0, 34-1, and OR gates 33-0 and 33-1 for generating a control signal to be applied to the other input terminal of the AND gates. The output of the OR gates is determined by the value set in two registers including a register 31 for setting redundant architecture and a register 30 for setting an active path.

In the case where each of the interface circuits 3-i and 3-(i+1) constituting the interface circuit pair accommodates a redundant transmission path, the value "0" indicating a "redundant architecture" is set in the register 31, and a value indicating a particular input signal wire constituting an active path is set in the register 30. In the case where the interface circuits 3-i, 3-(i+1) accommodate two nonredundant independent transmission paths, on the other hand, the value "1" indicating a "redundant architecture" is set in the register 31.

The relation between the values set in the two registers (including the register 31 for setting the redundant architecture and the register 30 for setting an active path) and the status of each of the two AND gates 32-0, 32-1 is shown in FIG. 7.

The following control operation is possible by changing the values set in the registers in response to an instruction